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DEVICE PERFORMANCE OF POLY-Si THIN-FILM TRANSISTORS FABRICATED ON YSZ CRYSTALLIZATION-INDUCTION LAYER VIA A TWO-STEP IRRADIATION METHOD USING PULSED LASER

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Abstract: In this study, we fabricated and investigated device performance of poly-Si thin-film transistors (TFTs) via a two-step pulsed-laser annealing (PLA) method on two kinds of substrates namely glass and YSZ*/glass. It was found that TFTs on YSZ/glass exhibited much better performance and uniformity among devices, e.g., they showed an average mobility of ~80 cm^2/Vs and standard deviation of ~18 cm^2/Vs, respectively, compared with ~40 cm^2/Vs and ~28 cm^2/Vs of TFTs on glass substrates, respectively. This result can be attributed to the better crystalline quality of the Si film on the YSZ/glass and the uniform distribution of grains as well as crystalline defects, which demonstrates the effectiveness of the crystallization-induction effect of the YSZ layer. (*YSZ: Yttria-Stabilized Zirconia)

Key words: PLA; solid-phase crystallization; low-temperature crystallization; silicon thin-film; YSZ; amorphous silicon; polycrystalline silicon.

1. Introduction

Low-temperature polycrystalline silicon (LT poly-Si) is a very attractive channel material for thin-film transistors (TFTs) due to its high stability or reliability and high mobility. Currently, LT poly-Si films are produced mainly by the excimer laser annealing (ELA) process, in which a-Si films deposited on glass substrates are melted and crystallized.[1-3] However, since random nucleation easily occurs due to melting-crystallization (MC), each grain size becomes random and the film surface gets rough, which leads to non-uniform electrical property in the whole substrate area. This limits extension of their application such as large display, active matrix organic light emitting diode (AM-OLED), etc. Further, ELA system needs a high cost due to frequent maintenance and is relatively unstable in operation. To overcome these issues, we have been studying the fabrication of LT poly-Si film by using YSZ $[(ZrO_2)_{1-x}(Y_2O_3)_x]$ crystallization-induction (CI) layer[4,5] and pulsed neodymium-doped yttrium aluminium garnet (Nd:YAG) (532 nm) laser annealing in solid-phase crystallization (SPC),[6,7] not MC. The SPC method can control the grain size roughly and reduce surface roughness much more, though the grain size becomes much smaller for rapid and high temperature annealing like PLA than MC method. Consequently, electrical property of the SPC film becomes poorer in general. However, we have already reported that with the two-step PLA method with the YSZ layer,[8-10] the crystalline quality gets much improved. Furthermore, by means of SPC, impurity activation can be performed simultaneously with crystallization, which reduces the process time for TFT fabrication effectively. The diffusion of impurity during SPC is negligible because of a very short annealing time of several ten ns. Also, the use of YAG laser instead of EL brings a reduction of cost as well-known.

In this paper, we present and compare characteristics of the poly-Si TFTs fabricated by pulsed Nd:YAG laser on the two substrates of glass and

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YSZ/glass, including the device-to-device uniformity in performance. From this result, we discuss the usefulness of the two-step PLA method with the YSZ-CI layer.

2. Experimental procedure

Figure 1 shows the schematic illustration for crystallization via the two-step method.[8,9] Firstly, a-Si films are irradiated at a low initial energy P_i to generate nuclei, followed by irradiation at a high growth energy P_g to accelerate the nuclei growth and film crystallization without random nucleation in the film bulk.

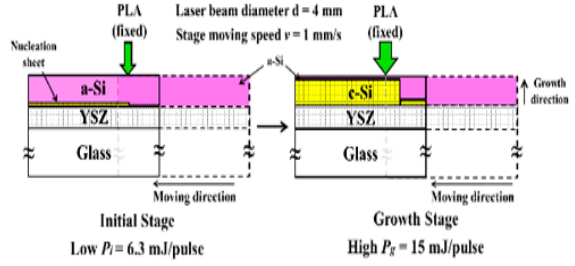

Figure 1. *Schematic illustration for crystallization by the two-step PLA method together with irradiation conditions*

For the fabrication of top-gate poly-Si TFTs, at first, a 60-nm-thick YSZ-CI layer is deposited on a glass substrate by reactive magnetron sputtering at the substrate temperature of 50 ^oC. The deposited YSZ layer has a (111)-preferred orientation. This is very favourable for Si crystallization growth because the YSZ layer acts as a crystallization-induction to control the orientation of crystallized Si film strongly. Then, an undoped 60-nm-thick a-Si film is deposited on a substrate (YSZ/glass or glass) by electron-beam evaporation. After that, a 50-nm-thick SiO_2 capping layer is deposited on the as-deposited a-Si film by atmospheric pressure chemical vapor deposition (APCVD) at 200 ^oC. The sample is then annealed in N_2 ambient at 350^oC for 30 min. After lithography patterning source and drain (S&D) regions, P ion implantation is performed with an acceleration voltage and an ion dose of 40~50 kV and $4.29\times10^{14} \sim 4.53\times10^{14}$ cm^{-2}, respectively. The average estimated doping concentration in the S&D regions is about 5×10^{19} cm^{-3}. Subsequently, the capping layer is removed before the crystallization of the a-Si film in a solid phase via the two-step method with a pulsed Nd:YAG laser (532 nm) together with activation of the implanted P ions in N_2 ambient. The diameter, repetition frequency, and pulse duration of the laser beam are 4 mm, 10 Hz, and 6-7 ns, respectively. During the laser irradiation, the sample is moved by a stage controller as shown in Fig. 1, where the moving speed is 1 mm/s and the moving distance per one shot is 100 µm. The initial laser energy P_i and growth laser energy P_g are set 6.3 and 15 mJ/pulse, respectively. After crystallization, Si islands are patterned, a 110-nm-thick SiO_2 gate oxide layer is deposited, and the contact holes for S&D are formed before the deposition of Al metal electrodes via vacuum evaporation. Finally, the sintering process is carried out at 350 ^oC in N_2 for 30 min. Characteristics of the fabricated TFTs are estimated by the precision semiconductor parameter analyzer 4156A. Figures 2(a) and (b) show a cross-sectional schematic illustration and top-view of the fabricated TFT. In this case, the number of used masks is 4.

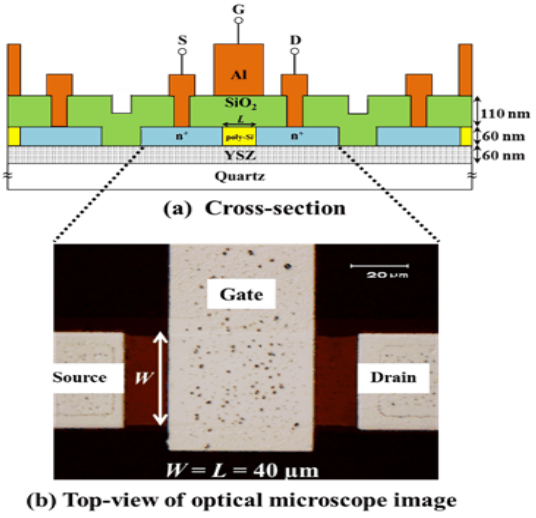

Figure 2. *(a) Cross-sectional schematic illustration and (b) top-view of optical microscope image of a fabricated poly-Si TFT*

3. Results and discussion

Figures 3(a) and (b) show typical transfer and output characteristics of the fabricated TFTs for the Si/glass structure with $W = L = 40$ µm. In Fig. 3(a), the transfer characteristic was measured at drain voltage $V_D = 0.1$ V. It can be seen that the TFTs can operate with

relatively small off leakage current of ~10^{-12} A. The gate leakage current is also smaller than the order of 10^{-10} A (the data are not shown). The ON/OFF ratio is in the order of 10^6. Also, the highest achieved electron field-effect mobility is ~40 $cm^2V^{-1}s^{-1}$. In Fig. 3(b), we can observe appropriate operation, though the linear and saturation regions are not obviously distinguished. This may be ascribed to ion drift in the gate oxide film. The details will be discussed later.

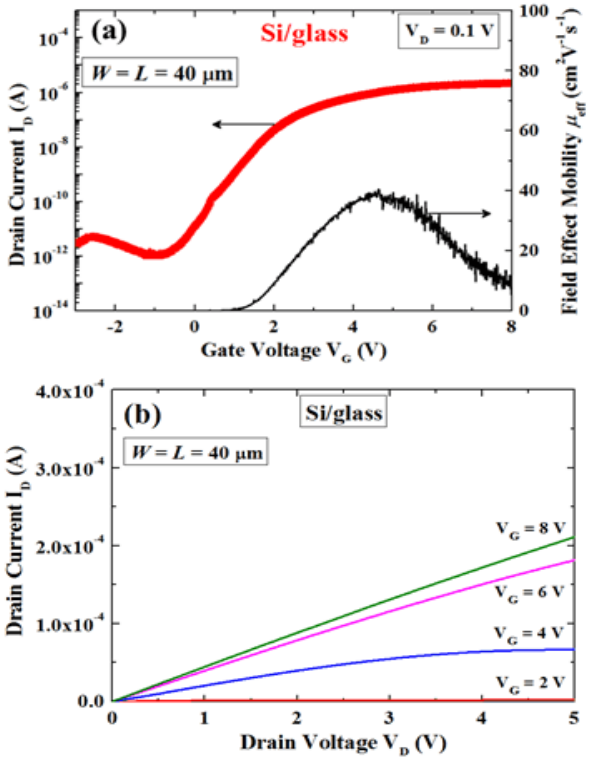

Figure 3. *(a) Transfer and (b) output characteristics of a fabricated poly-Si TFT for Si/glass structure with W = L = 40 μm*

Figures 4(a) and (b) show typical transfer and output characteristics of the fabricated TFTs for Si/YSZ/glass structure under the same condition as Fig. 3. From Fig. 3(a), it can also be seen that the TFTs can operate with a relatively small leakage current of ~10^{-12} A. The gate leakage current is also smaller than the order of 10^{-10} A (the data are not shown). The ON/OFF ratio is also in the order of 10^6. The highest achieved electron field effect mobility is up to 78 $cm^2V^{-1}s^{-1}$, twice higher than that for the Si/glass. From Fig. 4(b), we can also observe appropriate operation with higher drain currents than those of the Si/glass in Fig. 3(b). However, the linear and saturation regions are not also distinguished clearly like the case of Si/glass.

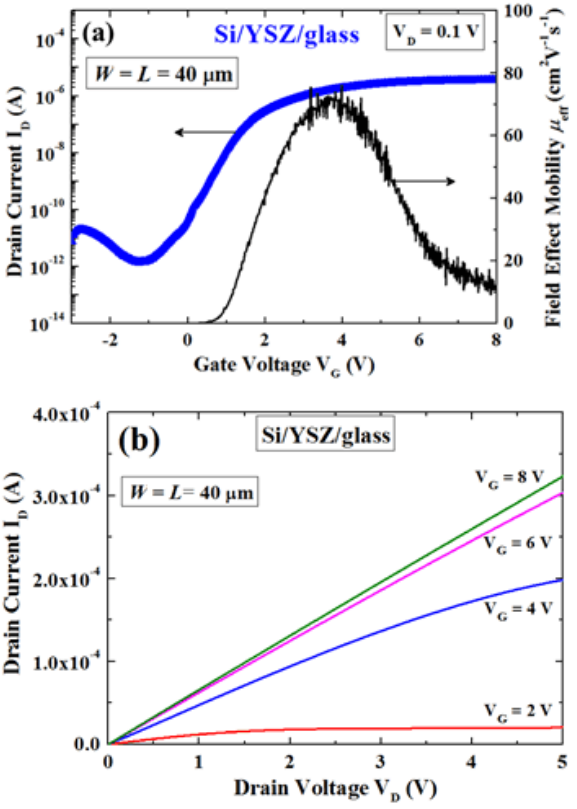

Figure 4. *(a) Transfer and (b) output characteristics of a fabricated poly-Si TFT for Si/YSZ/glass structure with W = L = 40 μm*

We estimated and summarized several important parameters of the device characteristics for the two structures of the Si/glass and Si/YSZ/glass. The field-effect mobility (μ_{eff}) and subthreshold swing (S.S) are evaluated from the linear and subthreshold regions, respectively, at V_D = 0.1 V. The ON/OFF current ratio is defined as the ratio of maximum drain current I_{Dmax} over minimum drain current I_{Dmin} within the measured range of I_D-V_G curve at V_D = 0.1 V. The threshold voltage (V_{th}) is determined by an interception of linear extrapolation of the I_D-V_G curve at V_D = 0.1 V. Table 1 summarizes the average values of device parameters together with their standard deviations of the TFTs with $W = L$ = 40 μm for the two structures. For each structure, 15 TFTs were measured. It can be seen that the TFTs fabricated on the YSZ/glass exhibit a higher μ_{eff} with smaller deviation than those on the glass. The

average V_{th} and average S.S of TFTs fabricated on the YSZ/glass are both smaller with smaller deviations than those on the glass. On the other hand, the average ON/OFF current ratio of TFTs fabricated on the YSZ/glass is almost similar to those on the glass. The field-effect mobility, threshold voltage, and subthreshold swing are strongly affected by the presence of grain boundaries and defects inside the channel. Therefore, it is considered that the better performance of the TFTs fabricated on the YSZ/glass are due to the better crystalline quality of the Si film on the YSZ/glass, comparing to that on the glass.[6,7] Also, the superior device-to-device uniformity in performance or smaller standard deviations of the TFTs fabricated on the YSZ/glass than on the glass is probably due to the more uniform grain size and crystalline defect distributions in the Si films for the former than for the latter substrate.[7-11]

We also observed a hysteresis phenomenon in the fabricated TFTs for the both structures of the Si/glass and Si/YSZ/glass. Figure 5 shows transfer characteristics of the TFTs with $W = L = 40$ µm fabricated on both the Si/glass and Si/YSZ/glass structures. In the measurements, the gate voltage was swept forward from -5 to 8 V, and then backward from 8 to -5 V. It can be seen clearly that the threshold voltages of backward sweeping (BS) curve shift to lower values than those of the forward sweeping (FS). The width of hysteresis for the Si/glass is a little larger than that for the Si/YSZ/glass. Further, the BS curve seems to show some improvement in subthreshold swing in comparison with the FS curve. At present, the reason for these hysteresises is not well known. In the C-V measurement, a hysteresis was observed in ion-drift type, which means the presence of mobile ions in the gate oxide. It is supposed that these mobile ions strongly affect the device performance of the fabricated TFTs and cause the hysteresis phenomenon. The drift ions are probably produced due to the low-temperature fabrication process of the gate oxide of SiO_2, since the low-temperature process sometimes brings imperfect structure, impurities, and unreacted ions in produced films. If the post-annealing is performed at a higher temperature, e.g., 400 °C, the hysteresis width might be reduced. Also, these drift ions affect TFTs output characteristics like Figs. 3(b) and 4(b). Pinch-off voltage V_p is expressed by $V_p = V_G - V_{th}$. If V_{th} is a negative value due to ion drift effect, V_p should be a large positive value. For example, when V_{th} is -3 V as shown in the dashed circle A region of Fig. 5, V_p is 7 V for $V_G = 4$ V, then, a linear region should be observed in TFT output characteristics like Figs. 3(b) and 4(b). But, if V_{th} is a positive value, we may observe a saturation region. We should further investigate to find causes for the hysteresis phenomenon clearly, including other unideal ones.

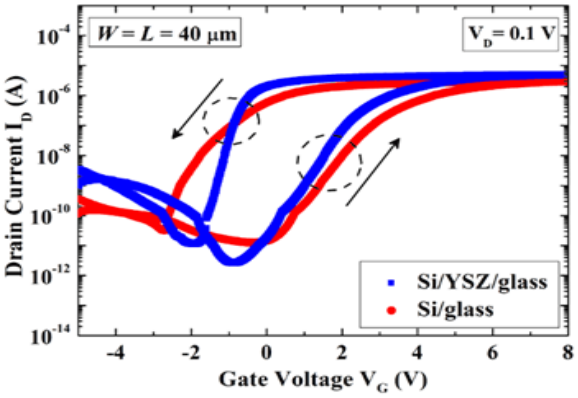

Figure 5. *Hysteresis phenomenon occurring in the transfer characteristics of fabricated poly-Si TFTs with $W = L = 40$ µm at $V_D = 0.1$ V for the two structures of the Si/glass and Si/YSZ/glass*

Table 1. *Average values of μ_{eff}, V_{th}, and S.S together with their standard deviations, and the average ON/OFF ratio of the TFTs with $W = L = 40$ µm for the two structures of the Si/glass and Si/YSZ/glass*

	Field-effect mobility μ_{eff} ($cm^2V^{-1}s^{-1}$)		Threshold voltage V_{th} (V)		Subthreshold swing S.S (mV/dec.)		ON/OFF ratio	
	Average value	Standard deviation	Average value	Standard deviation	Average value	Standard deviation	Average value	Standard deviation
Si/glass	40.3	28	2.83	0.78	426	99	1.74×10^6	1.08×10^6
Si/YSZ/glass	78.1	18	2	0.22	306	31	9.14×10^5	1.01×10^6

4. Conclusion

We fabricated poly-Si TFTs on both the substrates of glass and YSZ/glass. The device parameters of μ_{eff}, V_{th}, S.S, and ON/OFF current ratio of the fabricated TFTs were estimated as well as their uniformity. It was found that the TFTs fabricated on the YSZ/glass exhibit

better performance and device-to-device uniformity than those on the glass. This implies the better crystalline quality of the Si film and uniform distribution of grain size as well as crystalline defect on the YSZ/glass, compared to the glass, owing to the YSZ-CI layer and the two-step method. However, a hysteresis phenomenon was observed in the TFTs characteristics. Although the hysteresis mechanism is not well known at present, it might be related to the presence of mobile ions in the gate oxide. It is expected that with further improving annealing and fabrication conditions, the LT poly-Si film would be available for future application, e.g., AM-OLED.

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HIỆU SUẤT THIẾT BỊ CỦA TRASISTOR MÀNG MỎNG POLY-Si CHẾ TẠO TRÊN LỚP KÍCH THÍCH KẾT TINH YSZ BẰNG PHƯƠNG PHÁP NUNG HAI BƯỚC SỬ DỤNG LASER XUNG

Tóm tắt: Trong nghiên cứu này, chúng tôi đã chế tạo và khảo sát hiệu suất thiết bị của các transistor màng mỏng poly-Si bằng phương pháp nung hai bước sử dụng chùm laser xung trên hai loại đế là thuỷ tinh và YSZ/thuỷ tinh. Kết quả cho thấy các transistor màng mỏng trên đế YSZ/thuỷ tinh có hiệu suất và sự đồng đều giữa các thiết bị tốt hơn, ví dụ như độ linh động trung bình là ~80 cm^2/Vs và độ lệch chuẩn của nó là ~18 cm^2/Vs, so với ~40 cm^2/Vs và ~28 cm^2/Vs của các transistor màng mỏng trên đế thuỷ tinh. Kết quả này được coi là nhờ chất lượng tinh thể tốt hơn của màng Si trên đế YSZ/thủy tinh và sự phân bố đồng đều các hạt cũng như các khuyết tật tinh thể, thể hiện tính hiệu quả của hiệu ứng kích thích kết tinh của lớp YSZ. (*YSZ: Yttria-Stabilized Zirconia)

Từ khóa: PLA; kết tinh pha rắn; kết tinh nhiệt độ thấp; màng mỏng silic; YSZ; silic vô định hình; silic đa tinh thể.